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FRTRNS [part of paper # 10]

CERTIFICATION

I, Harumasa ISHIZAKI of FUSOH PATENT FIRM, Rindo Building, 5F, 37, Kanda-Higashimatsushita-cho, Chiyoda-ku, Tokyo, 101 Japan, hereby certify that I am the translator of the accompanying certified official copy of the patent application No.2000-016168 for a patent filed in Japan on January 25, 2000 and certify that the following is a true and correct translation to the best of my knowledge and belief.

Dated this 16th day of January 2003

H. Ishizaki

Harumasa Ishizaki

PATENT OFFICE
JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this Office.

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Commissioner,
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【LIST OF DOCUMENTS ATTACHED】

【NAME OF DOCUMENT】

SPECIFICATION.....1

【NAME OF DOCUMENT】

DRAWINGS.....1

【NAME OF DOCUMENT】

ABSTRACT.....1

【GENERAL POWER OF ATTORNEY NUMEBR】 9001716

【PROOF】 Requested

【NAME OF THE DOCUMENT】

【TITLE OF THE INVENTION】 CIRCUIT BOARD

【CLAIMS】

【Claim 1】 A circuit board comprising an interconnect layer having an externally exposed portion and a base member having a dielectric layer to cover an area except for the externally exposed portion,

between said dielectric layer and said base member, a electrically-floating conductive layer is formed for filling a space extending in a direction perpendicular to thickness of said interconnect layer with a specified gap

said electrically-floating conductive layer and said interconnect layer are disposed parallel to each other on the same plane.

【Claim 2】 The circuit board as defined in claim 1, wherein a pair of the interconnect layers are disposed on each of both surfaces of the base member.

【Claim 3】 The circuit board as defined in claim 2, wherein volumes of the pair of the interconnect layers are substantially same.

【Claim 4】 A circuit board comprising a base member having a first interconnect layer having an externally exposed

portion and a second interconnect layer disposed on the first interconnect layer via a dielectric layer on the same side of a surface,

a electrically-floating conductive layer formed for filling a space in the vicinity of said second interconnect layer under the dielectric layer on the base member,

said electrically-floating conductive layer and said first interconnect layer are disposed to overlap each other on the same plane.

【Claim 5】 A circuit board comprising an interconnect layer having an externally exposed portion and a base member having a dielectric layer and a die disposed thereon to cover an area except for the externally exposed portion,

a electrically-floating conductive layer is formed for filling a space in the vicinity of said interconnect layer under the dielectric layer of the base member,

said electrically-floating conductive layer and said die are disposed to overlap each other on the same plane.

【Claim 6】 The circuit board as defined in claims 1-5, wherein the interconnect layer includes patterns having a larger width.

【DETAILED DESCRIPTION OF THE INVENTION】

【0001】

【Field of the Invention】

The present invention relates to a circuit board preferably used in a semiconductor device such as having a land grid array (LGA) and a ball grid array (BGA).

【0002】

【Prior Art】

Recently, a multi-layered circuit board of higher integration is required for fabricating a semiconductor device package with smaller dimensions.

The circuit board for meeting the above requirement generally includes a base member mounting thereon a plurality of interconnect layers which sandwich dielectric layers therebetween.

【0003】

The base member includes a first and a second interconnect layers on the respective surfaces thereof, and the interconnect layers are connected with each other through a via-hole formed in the base member.

In such a circuit board, a relatively large part of the dielectric layer is externally exposed. When the circuit board is exposed to a higher humidity atmosphere, moisture enters into the rear surface of the dielectric layer through the externally exposed portion.

When the first and the second interconnect layers are formed by conductive materials having different coefficients of thermal expansion, a crack may be generated in the circuit board by the warp in case of a rapid temperature change.

【0004】

The above problem incurs lower reliability of such as having a lower packaging rank and failing in the temperature cycle test. In order to suppress the above problem, it is proposed that the interconnect layers and the dielectric layers be formed by materials having substantially same coefficients of thermal expansion or the thicknesses of the respective interconnect layers be increased

【0005】

However, the selection of the specific materials at the time of fabricating the circuit boars is burdensome and raises the cost. Further, the increased thickness makes the entire circuit board

larger not to meet the recent demand of the miniaturization.

【0006】

There are (1) JP-A-6(1994)-69212, (2) JP-A-7(1995)-154039, (3) JP-A-10(1998)-341077, (4) JP-A-11(1999)-154679 and (5) JP-A-11(1999)-260962 published as prior art.

【0007】

In the publications from (1)～(3), they describe "a circuit board including a dummy conductive film covering an interconnect conductive film with an intervention of a dielectric film", "a circuit board including a dummy conductive pattern formed in a dielectric region having a specific area larger than a circle having a radius of 1 mm", and "a circuit board including a dummy conductive layer covering an opening of a via-hole with an intervention of a dielectric film" respectively. Although each of the above publications describes suppression (prevention) of the crack generation, none of them describes a method for overcoming the ingress of the moisture into the rear surface of the dielectric layer.

【0008】

In the publication (4), "a circuit board including a dummy via-hole in the vicinity of a via-hole" is described. In the publication (5), "a circuit board including a dummy interconnect projected from a conductive interconnect" is described. Although each of these publications describes "the prevention of the film

peeling-off at the bottom surface of the via hole by dispersing a stress", and "the suppression of the increase of the thermal distortion by elevating the rigidity of the dielectric film", none of them describes "a method for overcoming the ingress of the moisture into the rear surface of the dielectric layer".

【0009】

In view of the foregoing, an object of the present invention is to provide a circuit board meeting the recent demand of the miniaturization and the reduction of cost in addition to satisfying the higher packaging rank and the temperature cycle test.

【0010】

【PROBLEM THAT THE INVENTION IS TO SOLVE】

In order to achieve the above object, a circuit board according to claim 1 comprises an interconnect layer having an externally exposed portion and a base member having a dielectric layer to cover an area except for the externally exposed portion,

between said dielectric layer and said base member, a electrically-floating conductive layer is formed for filling a space extending in a direction perpendicular to thickness of said interconnect layer with a specified gap

said electrically-floating conductive layer and said interconnect layer are disposed parallel to each other on the same plane.

Therefore, overall area of the base member is covered by the interconnect layer and the electrically-floating conductive

layer.

【0011】

According to claim 2 of the present invention, the circuit board as defined in claim 1, wherein a pair of the interconnect layers are disposed on each of both surfaces of the base member.

Therefore, almost entire area of the base member is covered by the interconnect layer and the electrically-floating conductive layer.

【0012】

According to claim 3 of the present invention, the circuit board as defined in claim 2, wherein volumes of the pair of the interconnect layers are substantially same.

Therefore, generation of warp of the base member caused by stress can be suppressed by the interconnect layer and the electrically-floating conductive layer.

【0013】

According to claim 4 of the present invention, a circuit board comprising a base member having a first interconnect layer having an externally exposed portion and a second interconnect layer disposed on the first interconnect layer via a dielectric layer on the same side of a surface,

a electrically-floating conductive layer formed for filling a space in the vicinity of said second interconnect layer under the

dielectric layer on the base member,

said electrically-floating conductive layer and said first interconnect layer are disposed to overlap each other on the same plane.

Therefore, generation of crack between the first interconnect layer and the base member can be suppressed by the electrically-floating conductive layer.

【0014】

According to claim 5 of the present invention, a circuit board comprising an interconnect layer having an externally exposed portion and a base member having a dielectric layer and a die disposed thereon to cover an area except for the externally exposed portion,

a electrically-floating conductive layer is formed for filling a space in the vicinity of said interconnect layer under the dielectric layer of the base member,

said electrically-floating conductive layer and said die are disposed to overlap each other on the same plane.

Therefore, generation of crack between the die and the base member can be suppressed by the electrically-floating conductive layer.

【0015】

According to claim 6 of the present invention,

interconnects of the interconnect pattern have a larger width.

Therefore, wider area of the base member can be covered by the interconnect layer having a larger width.

【0016】

【EMBODIMENTS OF THE INVENTION】

Now, the present invention is more specifically described with reference to accompanying drawings.

Fig.1 is a vertical sectional view showing a circuit board in accordance with a first embodiment of the present invention. Fig. 2 and Fig.3 are top and bottom plan views showing the circuit board of the first embodiment of the present invention. Fig.4 and Fig.5 are top and bottom plan views showing the circuit board of the first embodiment of the present invention after an interconnect layer and a electrically-floating conductive layer are formed.

In Figs.1 and 2, a circuit board (double layered interconnect structure) 1 includes an interconnect layer 3, a electrically-floating conductive layer (electrically-floating conductive layer) 4 and a dielectric layer 5 stacked on both surfaces of a base (core) element 2.

【0017】

The base member 2 is formed by a dielectric plate made of, for example, eposy resin having a plurality of penetrating holes 2a. The inner surfaces of the penetrating holes 2a are plated with a substance such as a metal using a catalyst for forming via-holes

6.

【0018】

The interconnect layer 3 includes a top interconnect layer 7 and a bottom interconnect layer 8 formed on the both surfaces of the base member 2, and parts of the interconnect layers 7, 8 are externally exposed. The surface of the interconnect layer 3 is chemically treated (surface-roughing) for elevating the bonding between the interconnect layer 3 and resin or solder resist.

【0019】

The top interconnect layer 7 is connected to an IC pad (not shown) through a bonding wire (not shown), and is formed by using interconnect patterns having a larger width as shown in Fig.4. Accordingly, a relatively larger surface area of the top surface of the base member 2 is covered with the top interconnect layer 7.

【0020】

The bottom interconnect layer 8 includes a land 9 which may be soldered to a system circuit board (not shown) and is connected to the via holes 6. The volume of the bottom interconnect layer 8 is adjusted to be the same as that of the top interconnect layer 7, thereby suppressing the generation of a stress due to the warp of the base member 2.

【0021】

When the surface areas of the both interconnect layers 7, 8 including the electrically-floating conductive layers are different

from each other, the thickness of the layers are adjusted such that the volumes of the both layers become identical.

When, for example, the layer areas of the top interconnect layer 7 and the bottom interconnect layer 18 are assumed to be 1 cm^2 and 0.8 cm^2, respectively, the thicknesses of the top interconnect layer 7 and the bottom interconnect layer 8 (t_1 and t_2) are determined such that an equation "$1 \times t_1 = 0.8 \times t_2$" is satisfied. Thereby, the warp of the circuit board (base member) 1 generated in the package fabrication step and influencing the conveyance can be suppressed and the warp stress generated in the interconnect layer 7 having the larger surface area can be reduced. Accordingly, the circuit board 1 can be fabricated having the higher packaging rank and the improved mass-productivity and reliability and satisfying the temperature cycle test.

【0022】

By the way, the packaging rank of the circuit board having the four-layered structure was measured and the circuit board was subjected to the temperature cycle test (-65℃ to 150℃). The packaging rank of the subject circuit board defined by JEDEC was "Level 3" while that of the conventional circuit board was "Level 5". The number of cycles endured by the subject circuit board was 500 while that of the conventional circuit board was less than 100.

【0023】

The electrically-floating conductive layer 4 includes a top

electrically-floating conductive layer 10 and a bottom electrically-floating conductive layer 11 formed on each of the surfaces of the base member 2.

【0024】

The surface of the electrically-floating conductive layer 4 is chemically treated (surface-roughing) for elevating the bonding between the electrically-floating conductive layer 4 and resin or solder resist. The top electrically-floating conductive layer 10 and the bottom electrically-floating conductive layer 11 are disposed between the base member 2 and a dielectric layer 5 such that the electrically-floating conductive layers 10, 11 fill space regions extending, with a specific interval, in directions perpendicular to the thicknesses of the top interconnect layer 7 and the bottom interconnect layer 8, respectively. Accordingly, the electrically-floating conductive layers 10, 11 do not exert an inverse effect such as short-circuit to the top interconnect layer 7 and the bottom interconnect layer 18, and cover almost all the surfaces of the base member 2. The top electrically-floating conductive layer 10 and the top interconnect layer 7 are disposed parallel to each other on the single plane, and the bottom electrically-floating conductive layer 11 and the bottom interconnect layer 8 are disposed parallel to each other on the single plane.

【0025】

The dielectric layer 5 includes a top dielectric layer 5a (for

example, solder resist) and a bottom dielectric layer 5b (for example, solder mask), which, respectively, cover the top interconnect layer 7 and the top electrically-floating conductive layer 10, and the bottom interconnect layer 8 and the bottom electrically-floating conductive layer 11, other than the exposed portions.

【0026】

An openings 12 for wire bonding pad is formed on the top dielectric layer 5a, and a resist mask 13 is formed on the periphery of the opening 12 in an upward projecting fashion.

The material used for die-mounting includes an Ag-paste-based material and a tape-shaped material. When the Ag-paste-based material is used, the resist mask 13 is applied twice for increasing the thickness, or the distance between the bonding pad (exposed portion of the top interconnect layer 7) and the die is sufficiently increased for preventing the short-circuit due to the exudation of the Ag-paste-based material.

An openings 14 for land bonding is formed on the bottom dielectric layer 5b.

【0027】

In the circuit board 1 thus fabricated, the ingress of the moisture into the rear (bottom) surface of the top dielectric surface 5a and into the rear (top) surface of the bottom dielectric surface 5b can be prevented. Further, the materials having coefficients of thermal expansion different from each other can be

used as those of the top interconnect layer 7 and bottom interconnect layer 8. Accordingly, the selection of the specific material is unnecessary different from the conventional circuit board fabrication.

In the first embodiment, the thickness of the entire circuit board can be reduced because the increase of the thickness of the interconnect layer is unnecessary for preventing the generation of the cracks in the circuit board.

【0028】

Although the interconnect pattern having the lager width is used in the top interconnect layer 7 in the first embodiment, the pattern width is not restricted thereto. As shown in Fig.6 illustrating a circuit board of a second embodiment, a top interconnect layer 61 can be formed by using an interconnect pattern having an ordinary width having no inverse effect on the high speed operation when the circuit board is used in a high speed semiconductor integrated circuit having no or little margin to operation speed.

【0029】

The number of the interconnect layers, the planer shape and the layout of the circuit board are not restricted to the first and second embodiments. As shown in Fig.7 illustrating a circuit board of a third embodiment, a top interconnect layer 71 having a shape with right angles may be used.

【0030】

As shown Fig.8 illustrating a circuit board of a fourth embodiment wherein the base member is given the same reference numeral as in Fig.1 and omitted detailed description, the circuit board 81 has a triple layered interconnect structure, that is, includes a top interconnect layer (not shown) on the top surface of the base member 2 having the same configuration as that of the first embodiment, and a first bottom interconnect layer 82 and a second bottom interconnect layer 83 on the bottom surface of the base member 2. The circuit board 81 further includes a electrically-floating conductive layer 84, a first dielectric layer 85 and a second dielectric layer 86.

【0031】

Part of the first bottom interconnect layer 82 is externally exposed for forming a land section 87.

The second bottom interconnect layer 83 is disposed overlying the first bottom interconnect layer 82 and the first dielectric layer 85 and sandwiching the second dielectric layer 86, or disposed between the base member 12 and the second dielectric layer 86.

【0032】

The electrically-floating conductive layer 84 and the first bottom interconnect layer 82 are disposed such that, if the electrically-floating conductive layer 84 does not exist, a portion (indicated by a chain line "A") in which a crack "C" is likely generated is sandwiched thereby and the electrically-floating

conductive layer 84 fills the space region near the second bottom interconnect layer 83. The electrically-floating conductive layer 84 and the second bottom interconnect layer 83 are disposed on the single plane.

【0033】

The first bottom interconnect layer 82 and the first dielectric layer 85 are disposed on the single plane.

The first dielectric layer 85 partially covers the first bottom interconnect layer 82 and sandwiches, with the electrically-floating conductive layer 84 and the second bottom interconnect layer 83, the second dielectric layer 86.

【0034】

In the circuit board thus configured, almost all the surfaces of the base member 2 are covered with the second bottom interconnect layer 83 and the electrically-floating conductive layer 84. Accordingly, the selection of the specific material is unnecessary similarly to the first embodiment.

In the present embodiment, the generation of the crack "C" in the second dielectric layer 86 between the base member 2 and the first dielectric layer 85 is suppressed by the presence of the electrically-floating conductive layer 84, or the electrically-floating conductive layer 84 acts as a crack stopper for the second dielectric layer 86. Accordingly, the thickness of the entire circuit board can be reduced similarly to the first embodiment.

【0035】

As shown Fig.9 illustrating a circuit board of a fifth embodiment wherein the base member is given the same reference numeral as in Fig.1 and omitted detailed description,, the circuit board 91 has a double layered interconnect structure, that is, includes an interconnect layer 92 and a die 93, and further includes a electrically-floating conductive layer 94 and a dielectric layer 95 overlying the base member 2 having the same configuration as that of the first embodiment.

【0036】

The interconnect layer 92 is layered on the base member 2 and part of the interconnect layer 92 is externally exposed.

The die 93 overlies the base member 2 and sandwiches, with the base member 2, the interconnect layer 92, the electrically-floating conductive layer 94 and the dielectric layer 95.

【0037】

The electrically-floating conductive layer 94 fills the space region near the interconnect layer 92 and is disposed such that, if the electrically-floating conductive layer 94 does not exist, a portion (indicated by a chain line "B") in which a crack "C" is likely generated is supported thereby. The electrically-floating conductive layer 94 and the interconnect layer 92 are disposed on the single plane.

The dielectric layer 95 covers part of the interconnect layer 92 and the whole electrically-floating conductive layer 94 between the base member 2 and the die 93.

【0038】

In the circuit board thus configured, almost all the surfaces of the base member 2 are covered with the interconnect layer 92 and the electrically-floating conductive layer 94. Accordingly, the selection of the specific material is unnecessary similarly to the first embodiment. In the present embodiment, the generation of the crack "C" in the dielectric layer 95 between the base member 2 and the die 93 is suppressed by the presence of the electrically-floating conductive layer 94. Accordingly, the thickness of the entire circuit board can be reduced similarly to the first embodiment.

【0039】

Since the above embodiments are described only for examples for the number of interconnect layers having two layers, three layers and four layers. However, the present invention is

not limited to the above embodiments and applicable for the interconnect layers having any layers.

【0040】

【EFFECT OF THE INVENTION】

According to the present invention, as described above, between said dielectric layer and said base member, a electrically-floating conductive layer is formed for filling a space extending in a direction perpendicular to thickness of said interconnect layer with a specified gap

said electrically-floating conductive layer and said interconnect layer are disposed parallel to each other on the same plane.

Therefore, almost an entire area of the base member is covered by the interconnect layer and the electrically-floating conductive layer.

【0041】

As a result, penetration of moisture into either of top and bottom dielectric layers can be prevented whereby the selection of the specific material is unnecessary and the cost can be lowered.

The thickness of the entire circuit board can be reduced because the thickness of the interconnect layer is unnecessary made larger for preventing from the generation of the cracks in the circuit board whereby recent requirements for a smaller and thinner product can be realized.

【BRIEF DESCRIPTION OF DRAWINGS】

【Fig.1】 A vertical sectional view showing a circuit board in accordance with a first embodiment of the present invention.

【Fig.2】 A top plan view showing the circuit board of the first embodiment of the present invention.

【Fig.3】 A bottom view showing the circuit board of the first embodiment of the present invention..

【Fig.4】 A top plan view showing the circuit board of the first embodiment of the present invention after an interconnect layer and a electrically-floating conductive layer are formed.

【Fig.5 】 A bottom view showing the circuit board of the first embodiment of the present invention after an interconnect layer and a electrically-floating conductive layer are formed.

【Fig.6】 A top plan view showing a circuit board in accordance with a second embodiment after an interconnect layer and a electrically-floating conductive layer are formed.

【Fig.7】 A top plan view showing a circuit board in accordance with a third embodiment after an interconnect layer and a electrically-floating conductive layer are formed.

【Fig.8】 A vertical sectional view showing a circuit board in

accordance with a fourth embodiment.

【Fig.9】 A vertical sectional view showing a circuit board in accordance with a fifth embodiment.

【EXPLANATION OF THE REFERENCE SYMBOLS】

1 circuit board

2 base member

2a through holes

3 interconnect layer

4 electrically-floating conductive layer

5, 5a, 5b dielectric surfaces

6 via holes

7 top interconnect layer

8 bottom interconnect layer

9 land

10 top electrically-floating conductive layer

11 bottom electrically-floating conductive layer

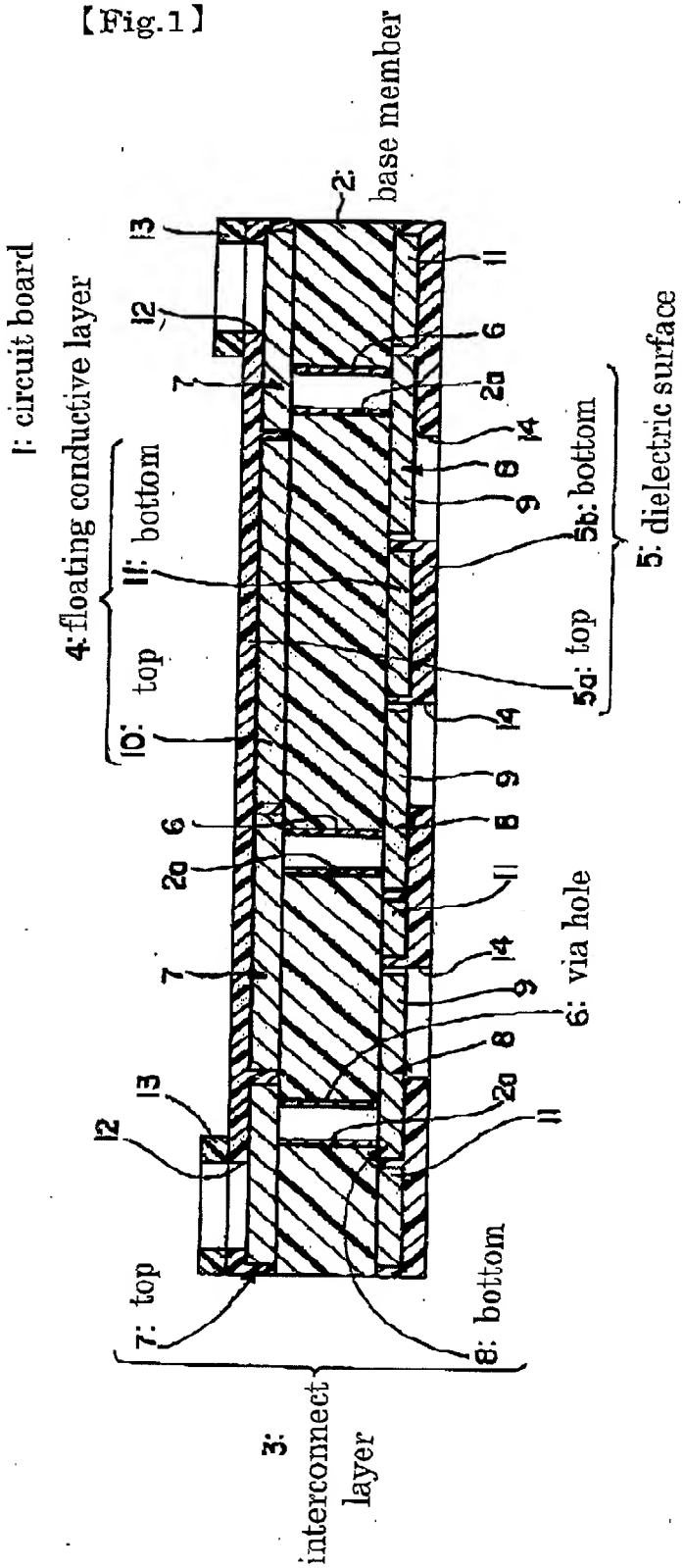
12 opening for wire bonding pad

13 resist mask

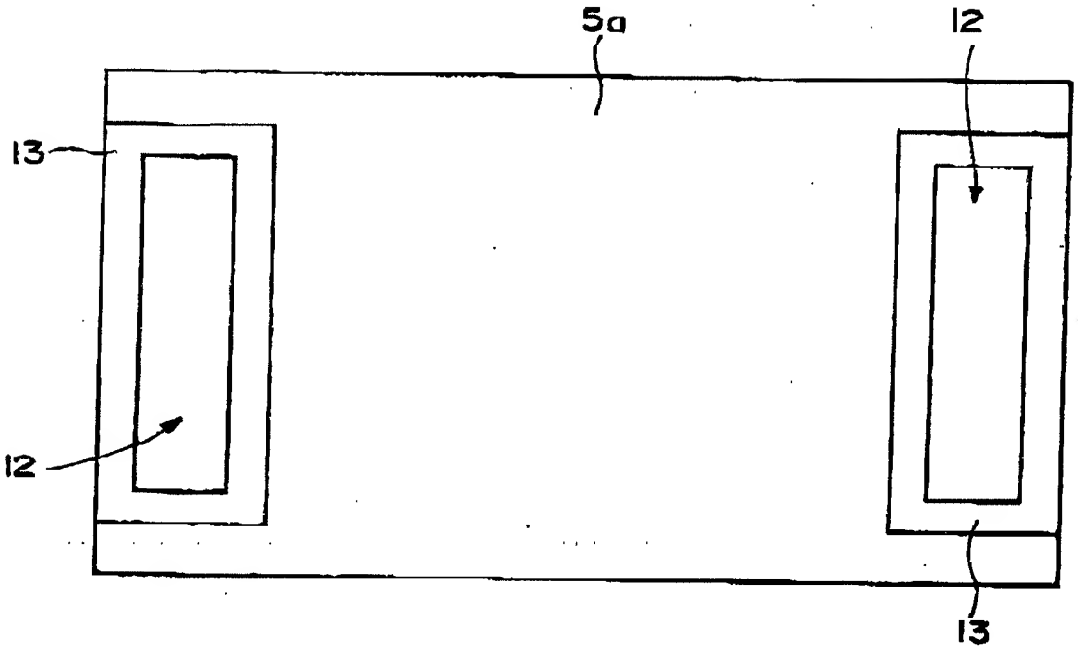
14 opening for land

【NAME OF THE DOCUMENT】 Drawings

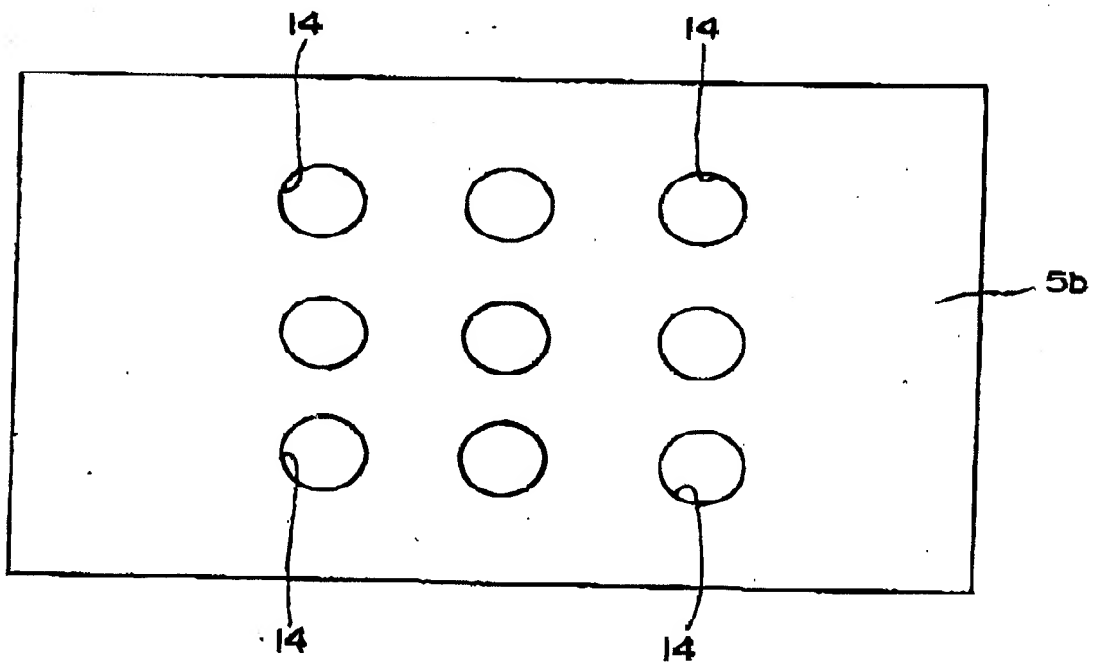
【Fig.1】



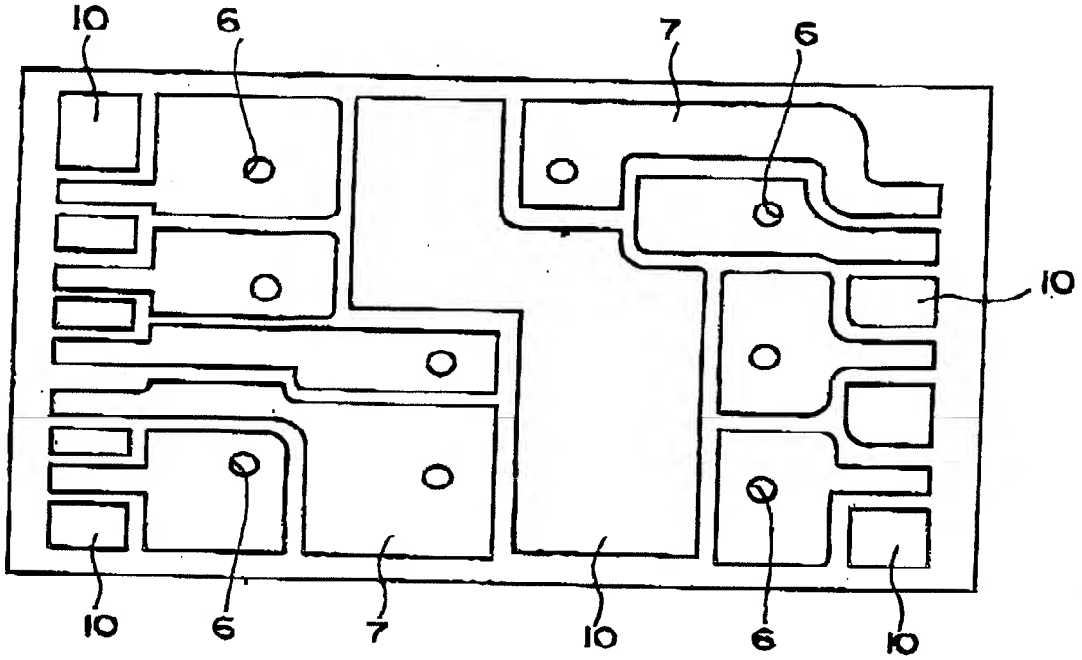
【Fig.2】



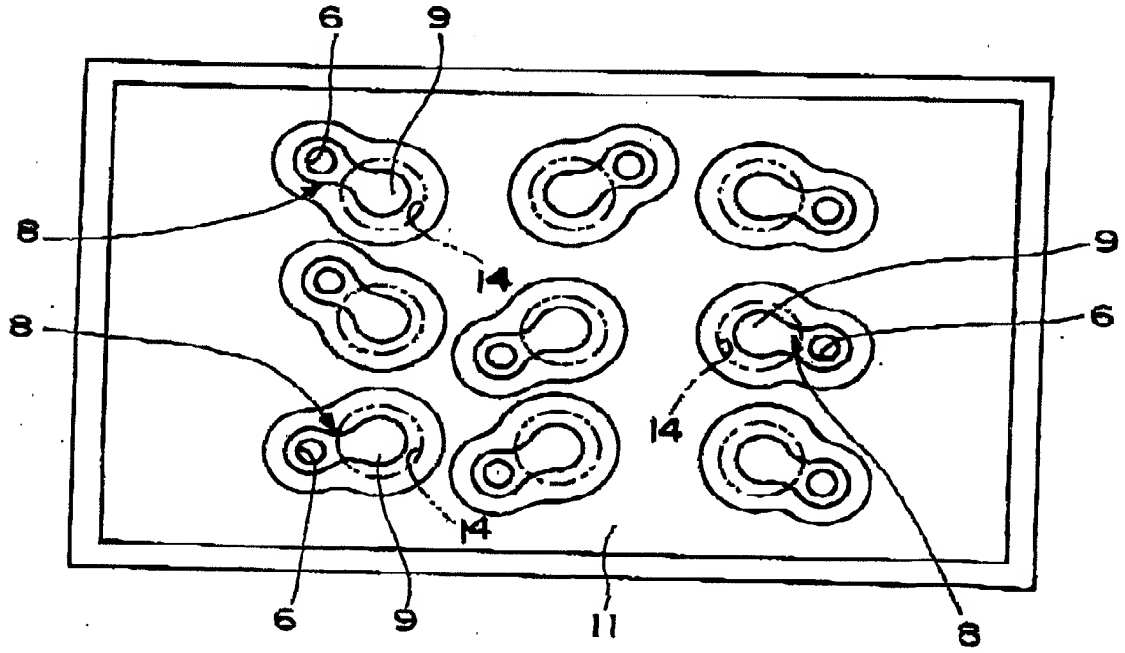
【Fig.3】



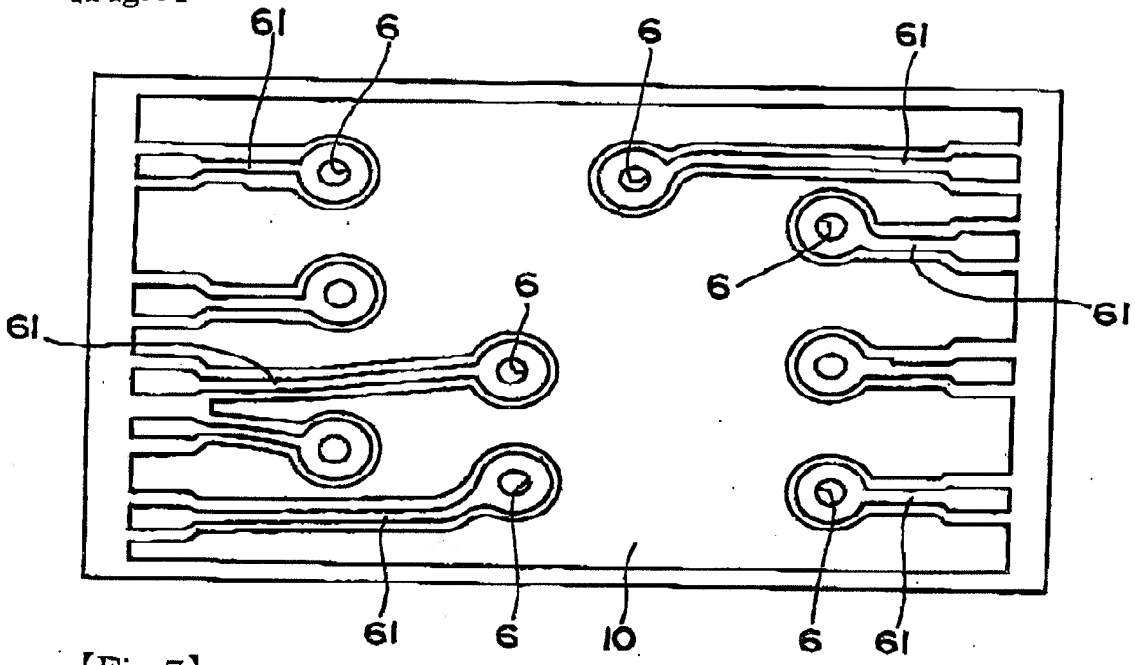
【Fig.4】



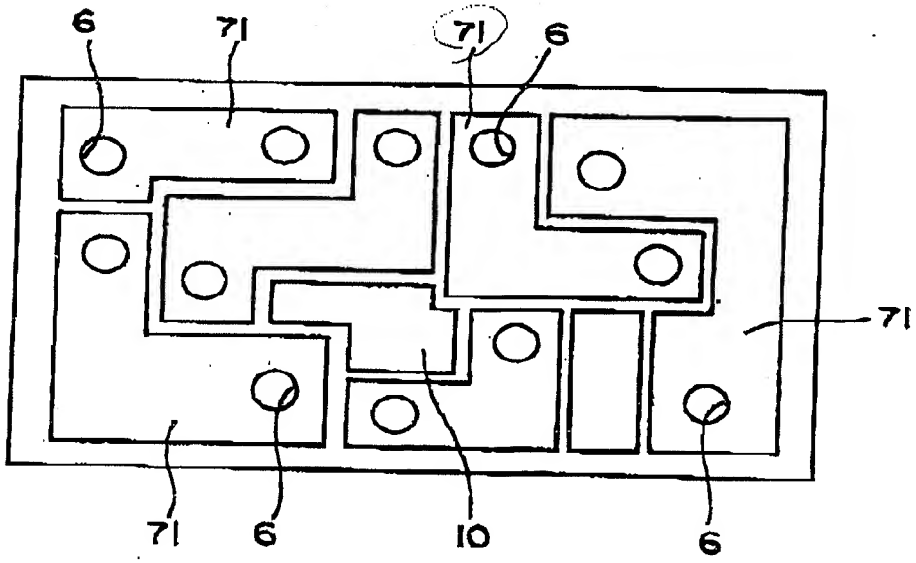
【Fig.5 】



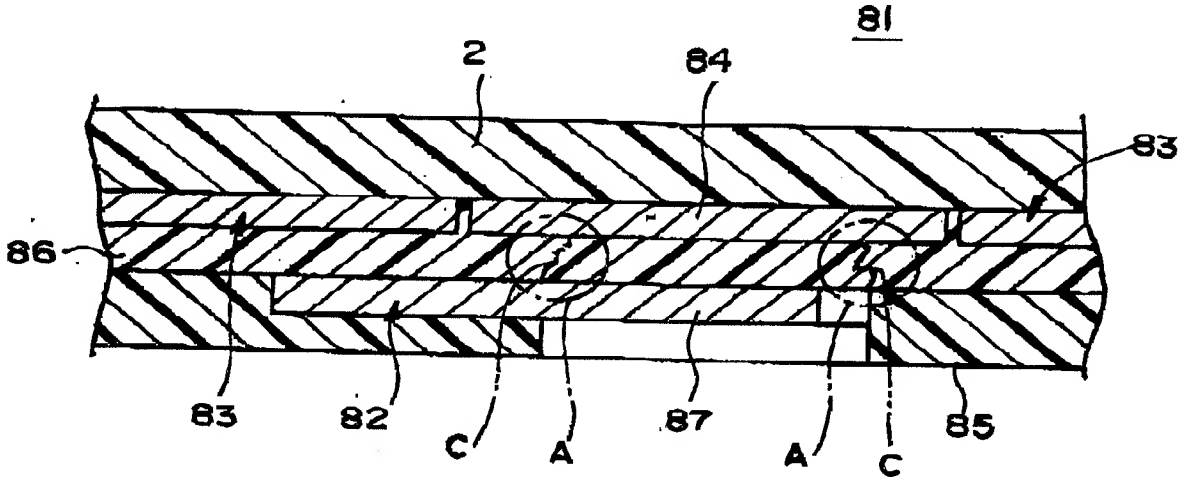
【Fig.6】



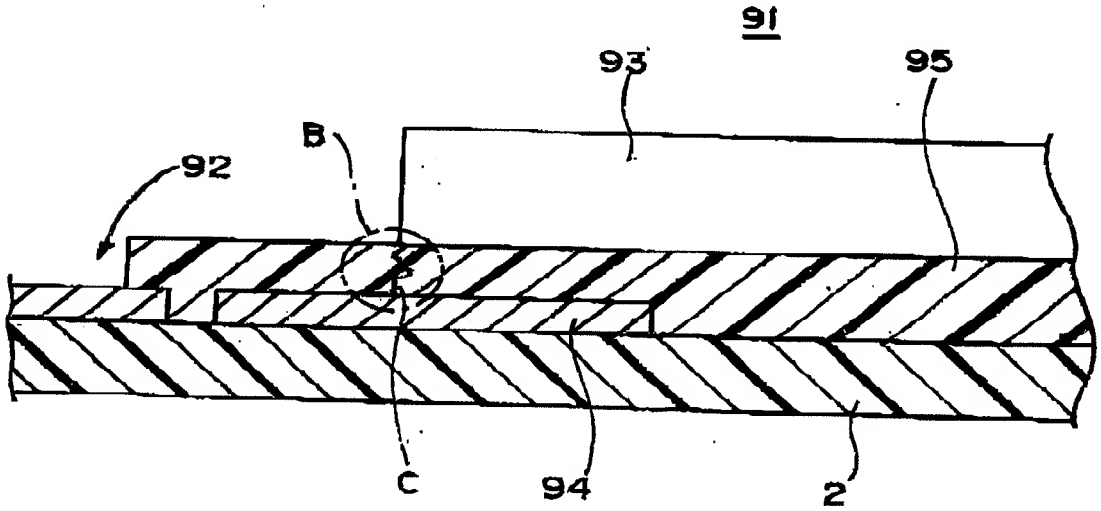
【Fig.7】



【Fig.8】



【Fig.9】



【NAME OF THE DOCUMENT】 ABSTRACT

【ABSTRACT】

【SUBJECT】 To lower cost and comply with recent requirements for smaller and thinner product.

【MEANS FOR SOLVING THE PROBLEM】

A circuit board comprising an interconnect layer 3 having an externally exposed portion and a base member 2 having a dielectric layer 5 to cover an area except for the externally exposed portion of the interconnect layer 3,

between said dielectric layer 5 and said base member 2, a electrically-floating conductive layer 4 is formed for filling a space extending in a direction perpendicular to thickness of said interconnect layer with a specified gap

said electrically-floating conductive layer 4 and said interconnect layer 3 are disposed parallel to each other on the same plane.

【SELECTED DRAWING】 Fig.1